Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A circuit board apparatus comprising:

a semiconductor package defined by a substrate having a matrix of conductive contact pads on both the top and bottom surfaces of the substrate; and

two interposers for receiving said semiconductor package, ~~the~~ each interposer defined by a body having a matrix of interposer contact bumps on both the inner and outer surfaces of the body, each interposer contact bump comprising an electrically conductive path and shaped to abut a contact pad of said semiconductor package and ~~contact pads of said PCB~~ a contact pad of a printed circuit board, wherein the inner surface of one of the interposers is adjacent to the top surface of the substrate and the inner surface of the other interposer is adjacent to the bottom surface of the substrate.

2. (Original) The apparatus of claim 1 wherein the contact pads of the semiconductor package are uniformly spaced.

3. (Original) The apparatus of claim 1 wherein the semiconductor package is a land grid array package.

4. (Currently amended) The apparatus of claim 1 wherein the contact ~~pads~~ bumps of ~~the interposer~~ at least one of the interposers are uniformly spaced.

5. (Original) The apparatus of claim 1 wherein the contact pads on the top surface of the semiconductor package support debugging and test operations.

6. (Original) The apparatus of claim 5 wherein the contact pads on the bottom surface of the semiconductor package are designated for production operations.

7. (Currently amended) A circuit board apparatus comprising:

a semiconductor package defined by a substrate having a matrix of conductive contact pads on both the top and bottom surfaces of the substrate; and

two interposers for receiving said semiconductor package, each interposer defined by a body having a matrix of interposer contact bumps on both the inner and outer surfaces of the body, each interposer contact bump comprising an electrically conductive path and shaped to abut a contact pad of said semiconductor package and a contact pad of a printed circuit board ~~The apparatus of claim 1~~ wherein the number of interposer contact ~~pads~~ bumps on the inner surface of ~~the interposer~~ at least one of the interposers exceeds the number of contact pads on the top surface of the semiconductor package.

8. (Currently amended) The apparatus of claim 1 wherein the interposer contact ~~pads~~ bumps on the inner surface of ~~the interposer~~ at least one of the interposers are arranged in the same pattern, pitch and spacing as the contact pads on the top surface of the semiconductor package.

9. (Currently amended) The apparatus of claim 8 wherein the semiconductor package contact pads have a 1.27 mm pitch or smaller.

10. (Original) The apparatus of claim 1 wherein the substrate supports 1443 signals to be collected.

11.-17. (Cancelled).

18. (Currently amended) A processor comprising:

a substrate having a matrix of conductive contact pads on the bottom surface of the substrate and a test port on the top surface of the substrate;

a first interposer disposed adjacent to the top surface of the substrate and coupled to the test port; and

a second interposer disposed adjacent to the bottom surface of the substrate and coupled to the conductive contact pads.

19. (Original) The processor of claim 18 wherein the test port comprises a conductive contact pad.

20. (Original) The processor of claim 18 wherein the test port is designated for debugging and test operations.

21. (Original) The processor of claim 18 wherein the contact pads on the bottom surface of the processor are designated for production operations.

22. (Original) The processor of claim 18 wherein the test port on the top surface of the substrate possesses approximately the same contact density as the contact pads on the bottom surface of the substrate.

23. (Original) The processor of claim 18 wherein the test port on the top surface of the substrate possesses approximately the same signal integrity as the contact pads on the bottom surface of the substrate.

24. (Original) The processor of claim 18 wherein the test port on the top surface of the substrate possesses approximately the same reliability as the contact pads on the bottom surface of the substrate.